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The 19th U.S.-Korea Forum on Nanotechnology

Vapour-deposited high-performance tin halide perovskite transistors

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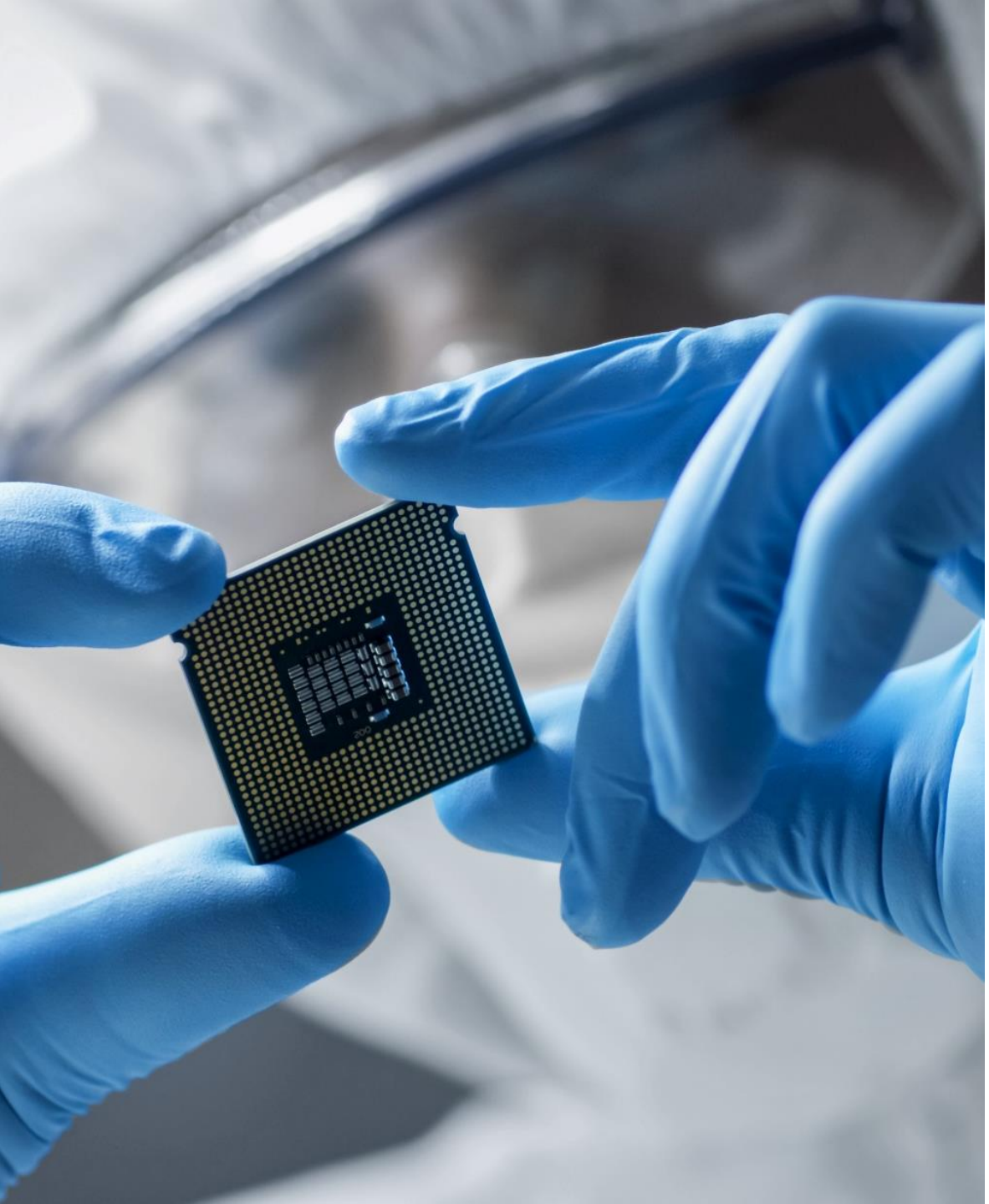

Outline

01 **Introduction:**
P-type semiconductors and tin perovskites

02 **Vapour-Deposited Perovskite TFTs**
High-quality thin-films and high-performance transistors

03 **Future Applications**
OLED backplane and M3D complementary circuits

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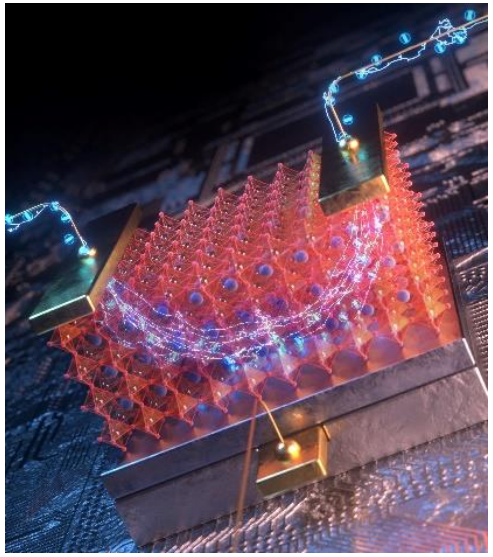
Ph.D. in Chemical Engineering, POSTECH

Advisor: Prof. Yong-Young Noh

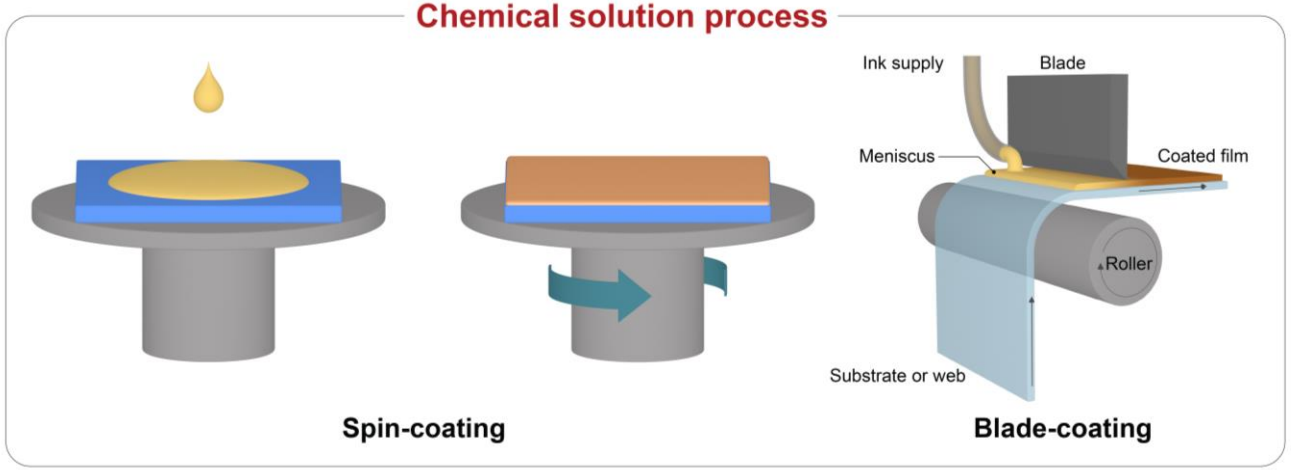
Doctoral Dissertation: Electrical Doping of Tin Halide Perovskites and Their Application in Transistors

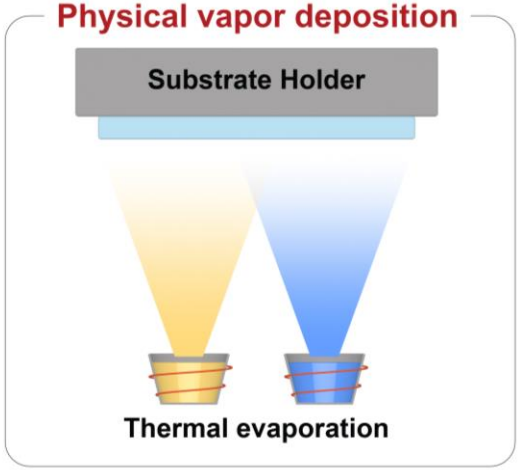
B.S. in Chemical Engineering, POSTECH

Main Research Topics

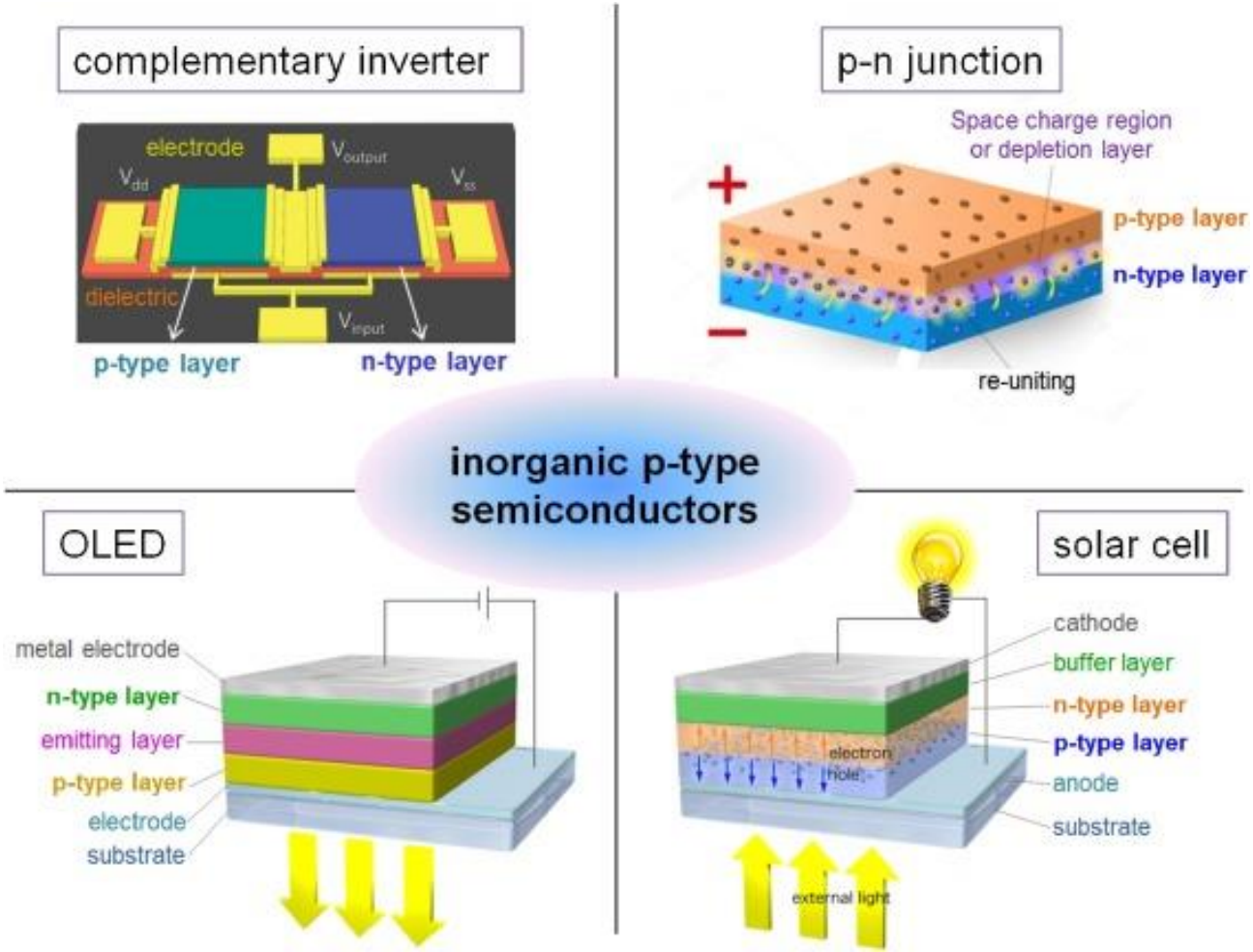


Perovskite transistors



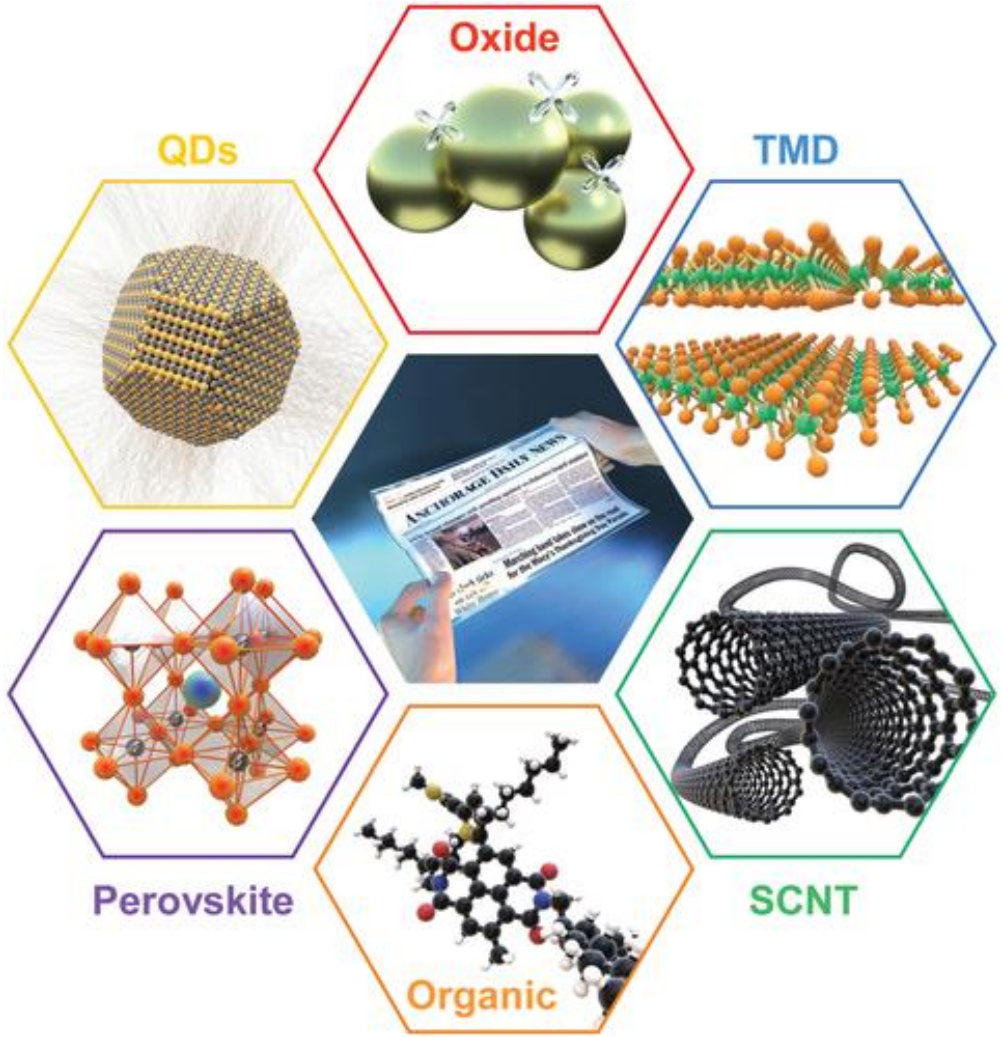


Why do we need p-type semiconductors?



Mat. Sci. Eng. R Rep. 135, 85-100 (2019).

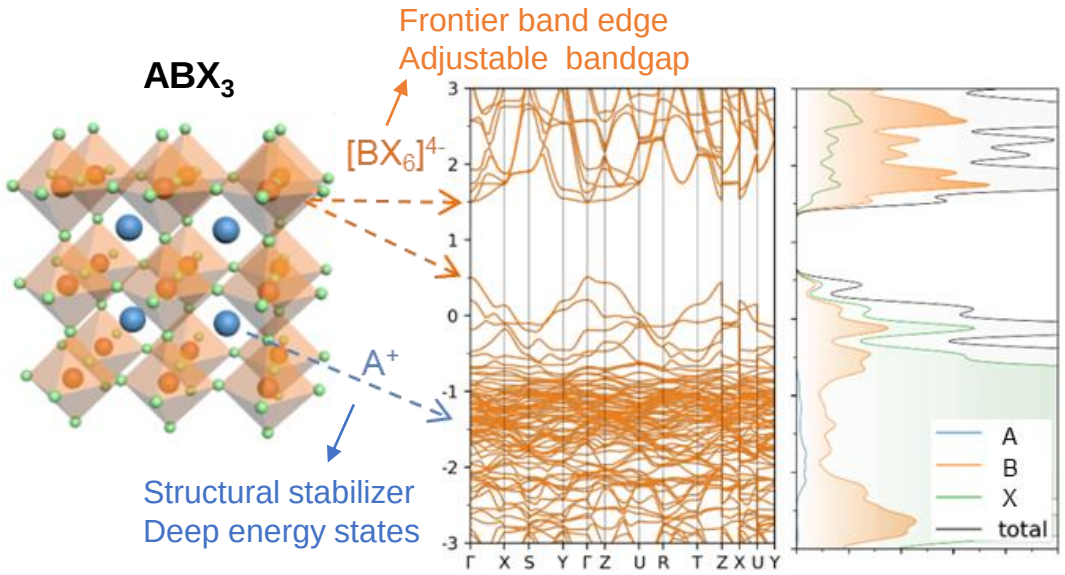
What type of materials are there?



Adv. Funct. Mater. 30(20), 1904588 (2020).

Tin Perovskites for P-channel TFTs

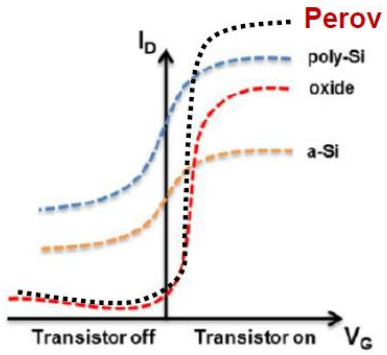
Excellent carrier transport material



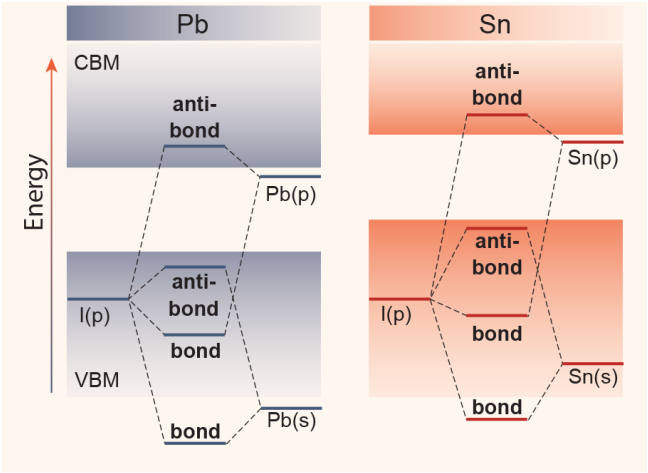
High mobility (μ)

$$\uparrow \mu = \frac{q\tau}{m^*\downarrow}$$

- Smaller effective mass
- Efficient charge carrier transport for high-performance transistor

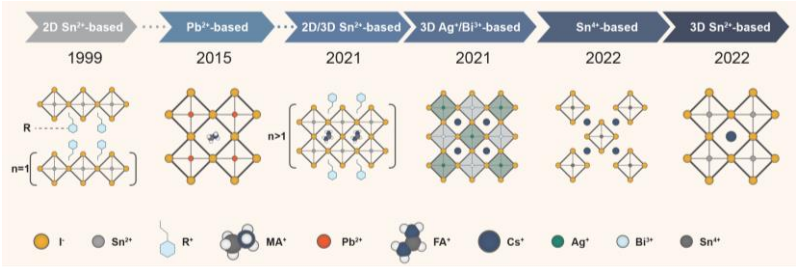


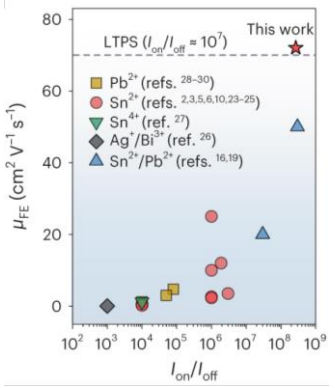
P-doped nature of tin perovskites



Tin perovskite for p-channel transistors

Heavily focused on solution-processed techniques





Adapted from Nat. Electron. 6, 559-571 (2023). Nat. Electron. 6, 650-657 (2023).

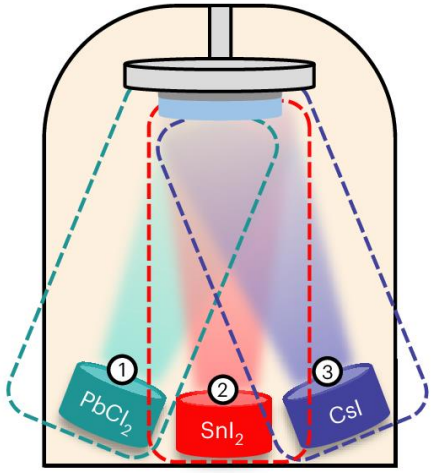
01

Introduction

Vapour-deposited Perovskite TFTs

Where this work stands

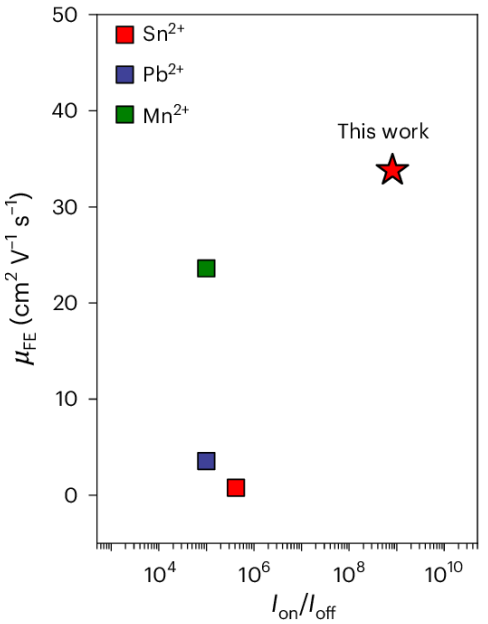
Choice of Perovskite Material



Cesium-tin-iodide

All inorganic metal halide perovskite

Channel material	$\mu_{FE,hole}$ ($cm^2\ V^{-1}\ s^{-1}$)	I_{on}/I_{off}	Device structure	Half life (days)	Ref.
$(C_6H_5C_2H_4NH_3)_2SnI_4$	0.78	~10^5	BGTC	--	2
$CH_3NH_3PbI_3$	3.55	~10^5	BGTC	--	3
$K_2MnCl_2I_2$	23.6	~10^5	BGTC	15	4
$K_2MnCl_2Br_2$	3.6	~10^3	BGTC	15	4
$CsSnI_3$:$PbCl_2$	33.8	~10^8	BGTC	> 150	this work



Fabrication of high-performance 3D tin halide perovskite TFTs

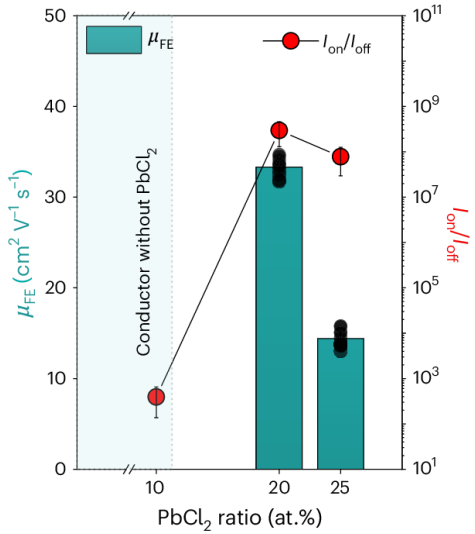
Average $\mu_{hole,\ FE}$ > 33.8 cm^2/Vs and I_{on}/I_{off} ~ 10^8

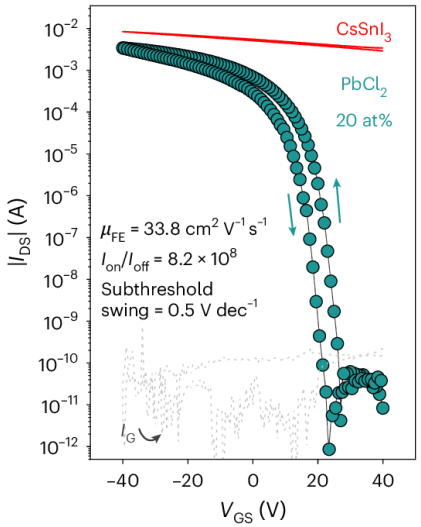
02

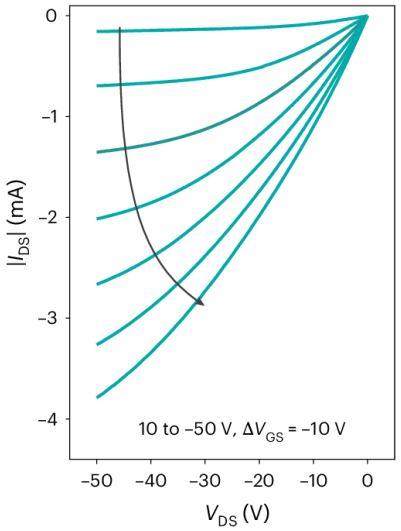
Results

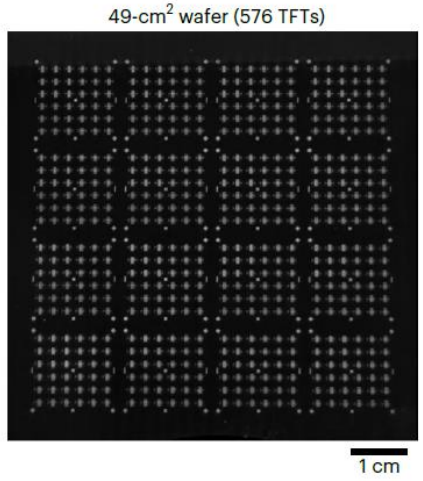
Optimized $CsSnI_3$:$PbCl_2$ TFT

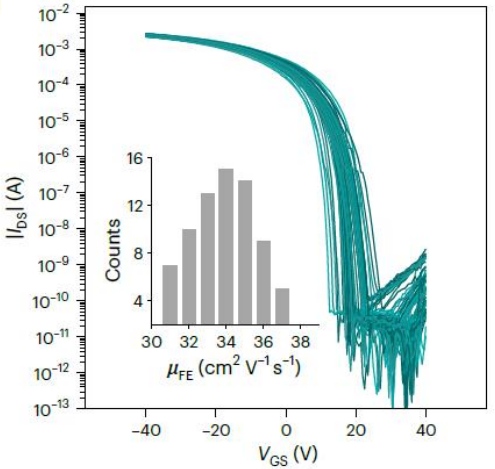
Electrical properties

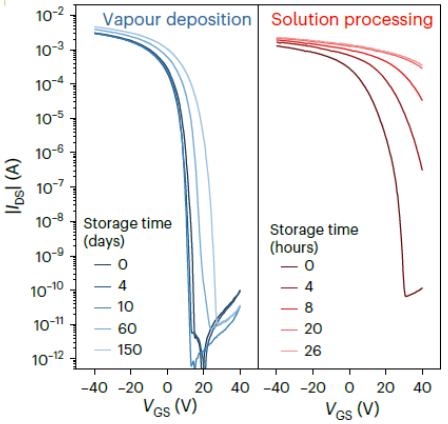


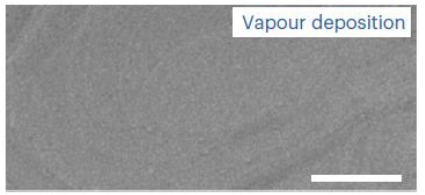


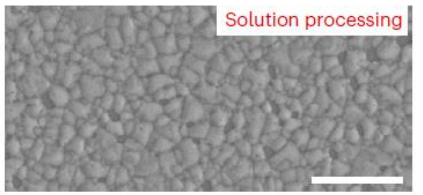












Successful modulation of hole concentration by $PbCl_2$

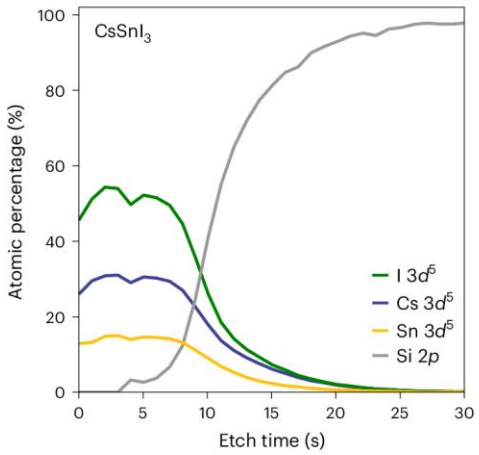
- $\mu_{FE,\ hole}$ ~ 33.8 cm^2/Vs and I_{on}/I_{off} ~ 10^8
- High storage stability: performance maintained without encapsulation beyond 150 days
- In comparison to solution-process with less than 24 hours of stability

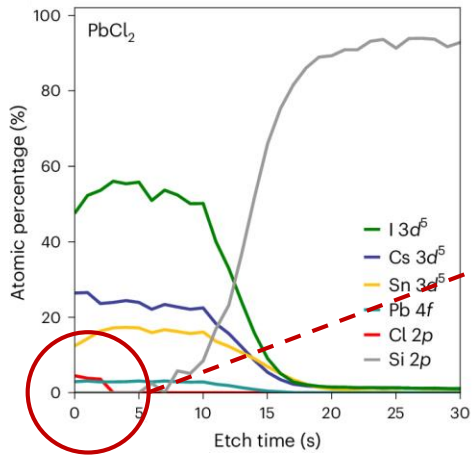
02

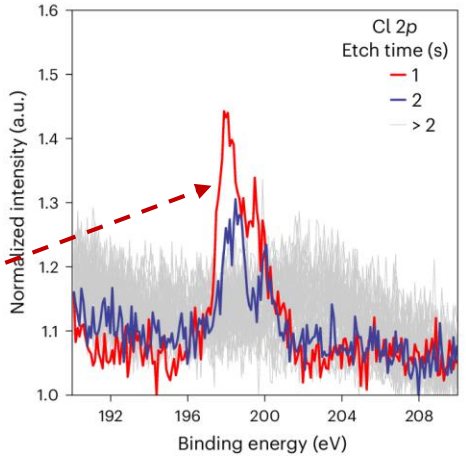
Results

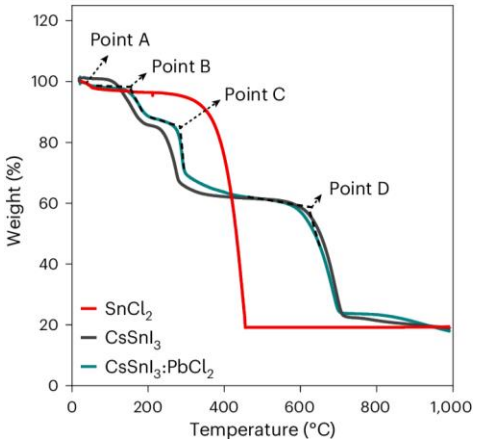
Distribution of Cl through Thin Film

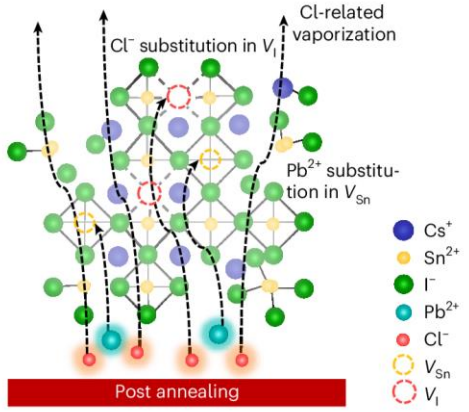
Where is Cl located?

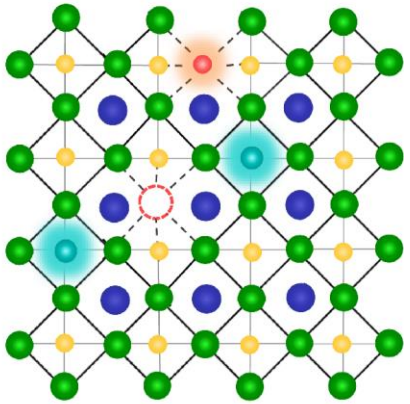












Post-annealed films

- Uniform distribution of all elements, except Cl

Dominant intrinsic defects

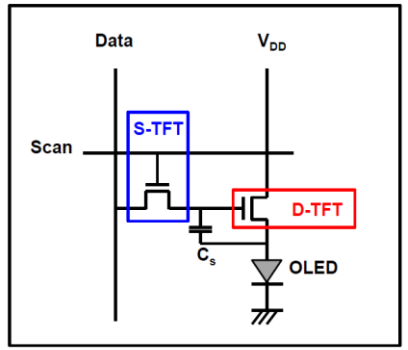
- V_{Sn}^{2-} (shallow acceptor: dominant native defect)
- V_I^{1+} (dominant compensating donor)

Lead(II) chloride can passivate these defects

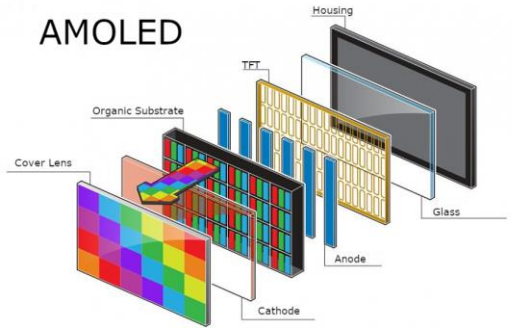
- Pb^{2+} takes place of V_{Sn} (hole source)
- After vaporization of Cl-related species: Trace Cl^- scattered or take place of V_I

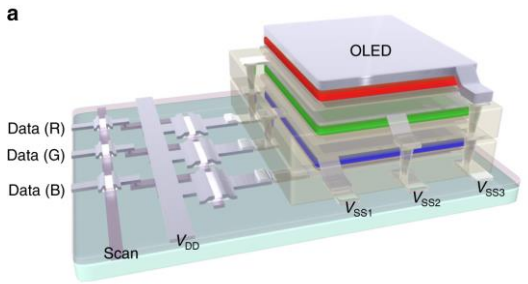
Application in One-Step Fabrication of OLED

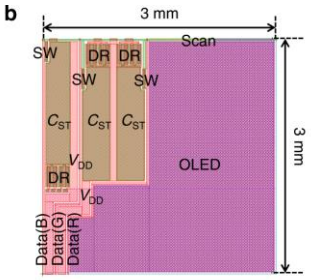
One-step, one-environment fabrication of TFT driven OLED



OLED pixel

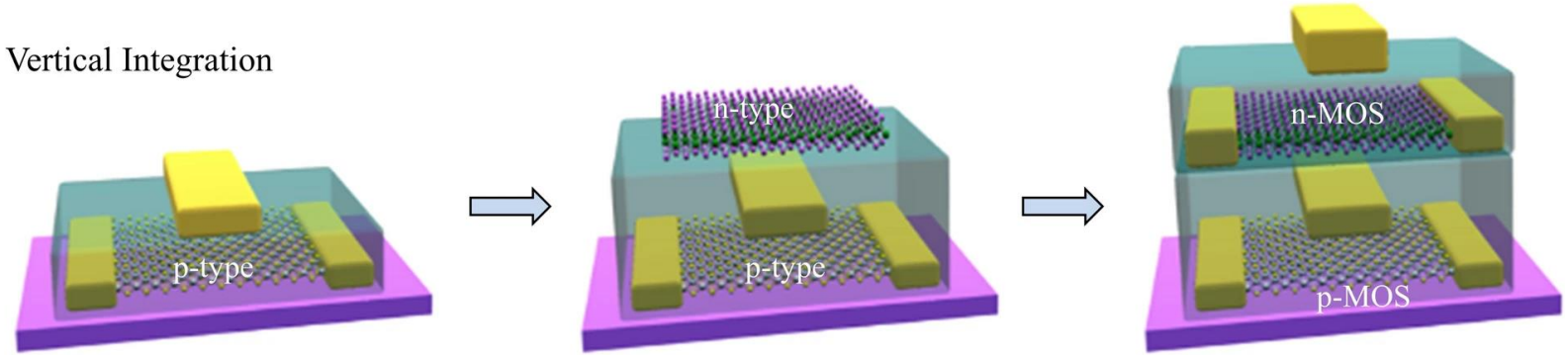






AOI Display. *Nat. Commun.* 11, 2732 (2022).

Vertical stack of driving TFT with OLED → Continuous thermal evaporation of each layer in one environment

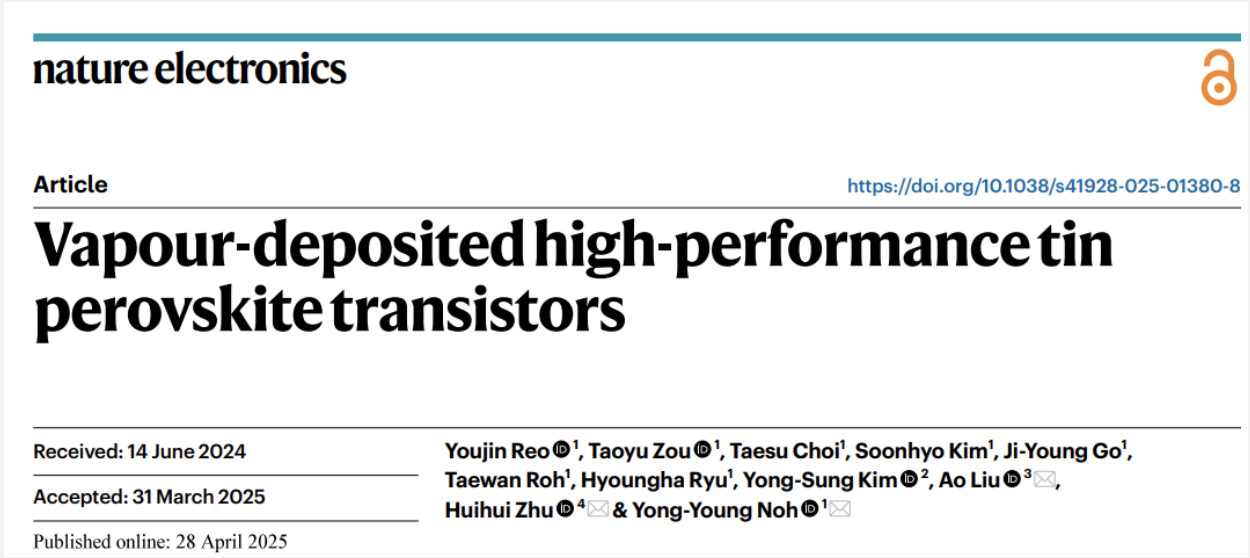


Nano Convergence 12, 11, (2025).

Vertical stack of p-type and n-type (e.g. In_2O_3, Bi_2Se_3 and more)

Summary

“Vapour-deposited high-performance p-type tin halide perovskite transistors”



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Article

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Vapour-deposited high-performance tin perovskite transistors

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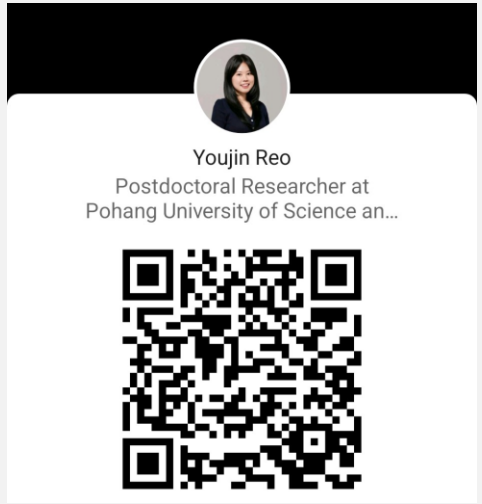
QR Code for Speaker’s LinkedIn



- $PbCl_2$: Hole suppressor and crystallization agent for high-quality thin-film with well-connected large grains
- Optimized TFT: record-high hole field-effect mobility over 33.8 cm^2/Vs, $I_{on}/I_{off} > 10^8$
- Successful large-area fabrication of high-performance metal halide perovskite transistors in an industry-compatible method, suitable for driving TFT in OLED backplane